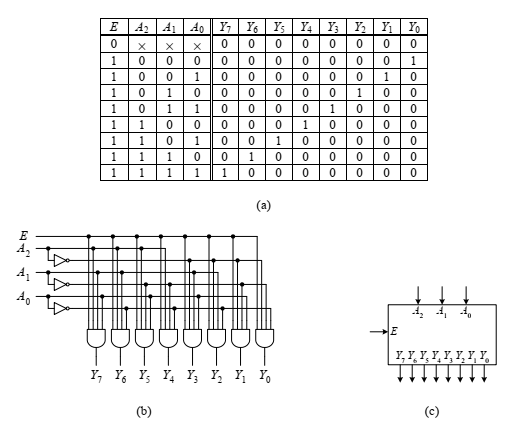
**Assignment 2**

**Note: All Verilog questions is developed basing on Structural modelling**

1. Write the Verilog module to implement 3-to-8 decoder, then develop the testbench to simulate and test this module. Show your simulation results



A 3-to-8 decoder: (a) truth table; (b) circuit; (c) logic symbol.

**Testbench.sv**

module decoder\_tb;

wire [7:0] out;

reg en;

reg [2:0] in;

integer i;

decoder3\_to\_8 dut(in,out,en);

initial begin

 $dumpfile("decoder\_tb.vcd");

$dumpvars(0, decoder\_tb);

 $monitor( "en=%b, in=%d, out=%b ", en, in, out);

   for ( i=0; i<16; i=i+1)

        begin

           {en,in}  = i;

            #1;

        end

end

endmodule

**Design.sv**

module decoder3\_to\_8( in,out, en);

input [2:0]  in;

input en;

output [7:0] out;

  reg [7:0] out;

 always @( in or en)

    begin

      if (en)

        begin

          out=8'd0;

          case (in)

              3'b000: out[0]=1'b1;

              3'b001: out[1]=1'b1;

              3'b010: out[2]=1'b1;

              3'b011: out[3]=1'b1;

              3'b100: out[4]=1'b1;

              3'b101: out[5]=1'b1;

              3'b110: out[6]=1'b1;

              3'b111: out[7]=1'b1;

              default: out=8'd0;

          endcase

      end

else

out=8'd0;

end

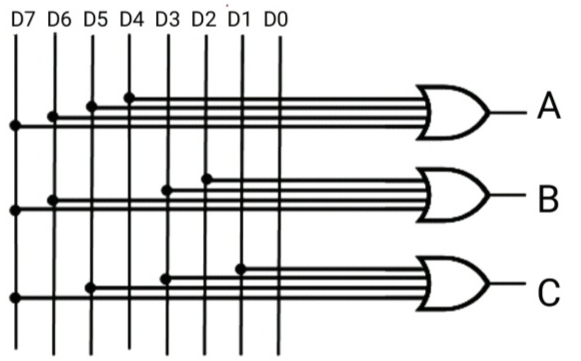
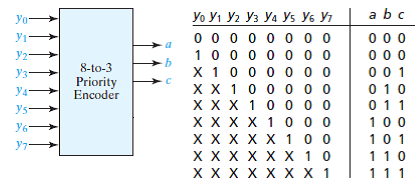
endmodule

A screenshot of a computer

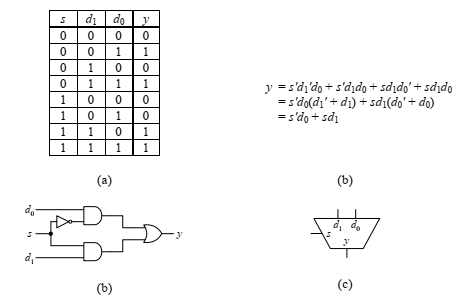
Description automatically generated A screenshot of a computer

Description automatically generated

1. Write the Verilog module to implement the 8-to-3 Priority encoder, then develop the testbench to simulate and test this module.

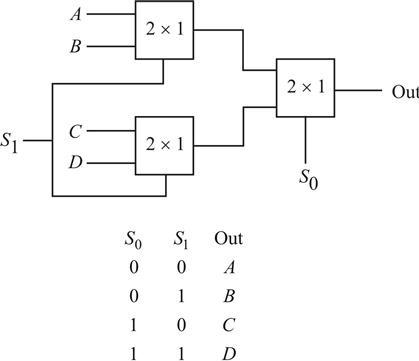


1. Write the Verilog module to implement An 2-to-1 multiplexer, develop the testbench to simulate and test this module.

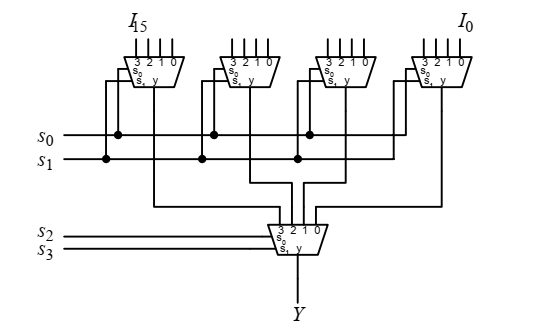


A 2-to-1 multiplexer: (a) truth table; (b) equation; (c) circuit; (d) logic symbol.

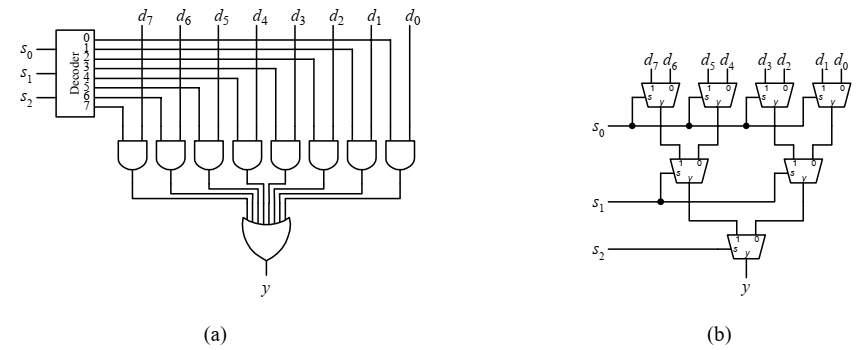
1. Write the Verilog module to implement the 4-to-1 multiplexer from three 2-to-1 multiplexer, then develop the testbench to simulate and test this module.



1. Write the Verilog module to implement 16-to-1 multiplexer using only 4-to-1 multiplexers, then develop the testbench to simulate and test this module.

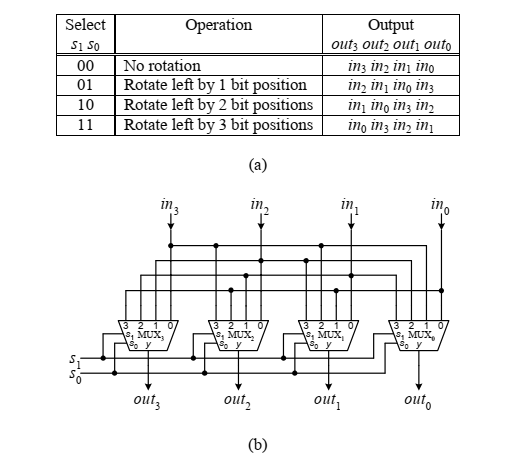


1. Write the Verilog module to implement the 8-to-1 multiplexer using 3-to-8 decoder method and using seven 2-to-1 multiplexers method. Develop the testbench to simulate and compare the operation of these two modules.



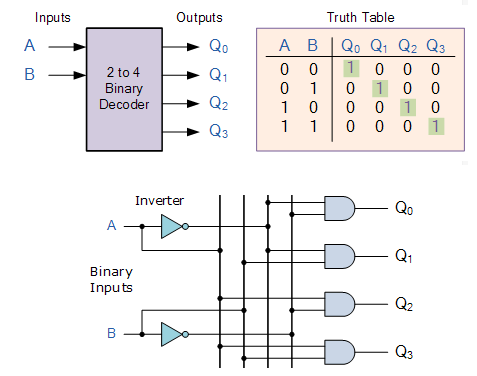
An 8-to-1 multiplexer implemented using: (a) a 3-to-8 decoder; (b) seven 2-to-1 multiplexers.

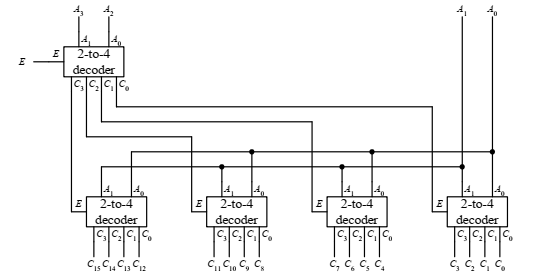
1. Write the Verilog module to implement 4-bit barrel shifter for the rotate left operation, then develop the testbench to simulate and test this module.



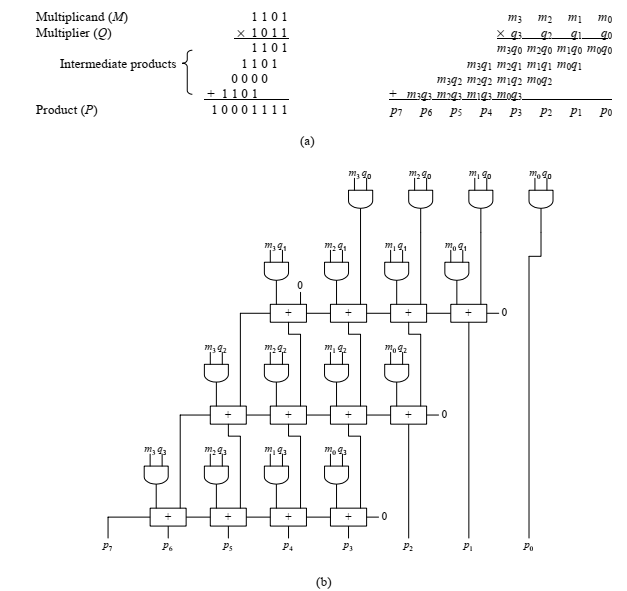
A 4-bit barrel shifter for the rotate left operation: (a) operation table; (b) circuit.

1. Write the Verilog module to implement 2-to-4 decoder, then develop the testbench to simulate and test this module.



1. Write the Verilog module to implement 4-to-16 decoder using only 2-to-4 decoders, then develop the testbench to simulate and test this module.

the circuit for the 4-to-16 decoder using only 2-to-4 decoders.

1. Write the Verilog module to implement 4 bit Multiplication circuit, then develop the testbench to simulate and test this module.

Multiplication: (a) method; (b) circuit.